

## CLAIMS

What is claimed is:

1. An embedded dynamic random access memory (DRAM) comprising:  
a metal oxide semiconductor (MOS) capacitor having a storage node formed between a P+ doped region and a polysilicon plate; and,  
an N- doped region by adding an extra P-type implantation which is substantially completely under the polysilicon plate and substantially under the P+ doped region, to decrease a threshold voltage of the capacitor and degrading the gradient of the PN junction doping profile between storage node and N-Well.
2. The embedded DRAM of claim 1, further comprising an N well in which the P+ doped region and the N- doped region are situated, the polysilicon plate situated over the N well.
3. The embedded DRAM of claim 2, wherein the N well is biased negative at a voltage Vdd.
4. The embedded DRAM of claim 1, further comprising a second P+ doped region.
5. The embedded DRAM of claim 4, further comprising a transfer gate over and between the P+ doped region and the second P+ doped region.

67,200-968  
2002-0397

6. The embedded DRAM of claim 5, wherein the transfer gate has applied thereto a  $V_{bb}$  turn-on voltage to turn on the embedded DRAM and a  $V_{pp}$  turn-off voltage to turn off the embedded DRAM.
7. The embedded DRAM of claim 1, wherein the MOS capacitor has a junction leakage current that is decreased due to the degraded PN junction doping profile resulted from the N- doped region.
8. The embedded DRAM of claim 1, wherein the N-doped region is formed by adding extra P-type dosages in N-Well region beneath the MOS capacitor or just using native N-Well implant without any  $V_t$  adjustment, pocket or channel implant.
9. The embedded DRAM of claim 1, wherein the MOS capacitor has a threshold voltage that is decreased due to the N- doped region.
10. The embedded DRAM of claim 1, wherein the N- doped region is fabricated at least in part by using an existing semiconductor mask.

✓

11. An embedded dynamic random access memory (DRAM) comprising:
  - an N well biased at a negative voltage;
  - a metal oxide semiconductor (MOS) capacitor having a storage node formed between a P+ doped region in the N well and a polysilicon plate over the N well; and,
  - a N- doped region in the N well substantially completely under the polysilicon plate and substantially under the P+ doped region, to increase a retention time of the storage node of the capacitor.
12. The embedded DRAM of claim 11, further comprising a second P+ doped region in the N well.
13. The embedded DRAM of claim 12, further comprising a transfer gate over and between the P+ doped region and the second P+ doped region.
14. The embedded DRAM of claim 13, wherein the transfer gate has applied thereto a V<sub>bb</sub> turn-on voltage to turn on the embedded DRAM and a V<sub>pp</sub> turn-off voltage to turn off the embedded DRAM.
15. The embedded DRAM of claim 11, wherein the MOS capacitor has a junction leakage current that is decreased due to the N- doped region.

67,200-968  
2002-0397

16. The embedded DRAM of claim 11, wherein the MOS capacitor has a threshold voltage that is decreased due to the N- doped region.

17. The embedded DRAM of claim 11, wherein the N- doped region is fabricated at least in part by using an existing semiconductor mask.

18. A method comprising:

fabricating a metal oxide semiconductor (MOS) capacitor of an embedded dynamic random access memory (DRAM) having a storage node formed between a P+ doped region and a polysilicon plate; and,

N- doping a region substantially completely under the polysilicon plate and substantially under the P+ doped region, to increase a retention time of the storage node of the capacitor.

19. The method of claim 18, wherein the MOS capacitor has a junction leakage current that is decreased due to the N- doped region.

20. The method of claim 18, wherein the MOS capacitor has a threshold voltage that is decreased due to the N- doped region.

67,200-968  
2002-0397

21. The method of claim 18, wherein the N- doped region is fabricated at least in part by using a semiconductor mask used in fabricating the MOS capacitor.